VITERBI DECODER
Application Notes

Rev. [6/2012]

6-19-2012

Table of Contents

GENERAL DESCRIPTION 3
FEATURES 3
FUNCTIONAL DESCRIPTION 4
INTERFACE 5
Symbol 5
Signal description 5
Typical Core Interconnection 6
IMPLEMENTATION DATA 6
Performance 6

GENERAL DESCRIPTION

Viterbi encoding is widely used for satellite and other noisy communications channels. There are two important components of a channel using Viterbi encoding:

- the Viterbi encoder (at the transmitter),
- the Viterbi decoder (at the receiver).

A Viterbi encoder adds extra information in the transmitted signal to reduce the probability of errors in the received signal that may be corrupted by noise.

A Viterbi decoder performs a maximum likelihood detection of 1 bit data transmitted over a channel with inter-symbol interference (ISI). The 1-bit data to be transmitted is encoded with an n-bit convolutional code in the convolutional encoder. The following figure shows the simplified data path from the Convolutional Encoder to the Viterbi Decoder.

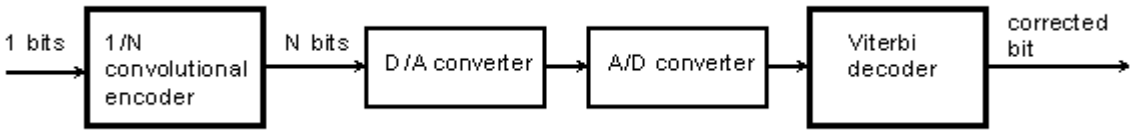

Figure 1. Simplified data path from the Convolutional Encoder to the Viterbi Decoder.

Viterbi encoding (convolutional encoding)applied in:

- wireless telecommunication:
  - digital cellular phones
  - satellites
  - satellite ground stations
- consumer electronics
  - CD players
  - HDTVs.

FEATURES

- Decoding of convolutional codes,
- Hard Decision Decoding,
- Trace-back method for survivor memory,
- Parameterized architecture allows for customization of the following functions:
  - Convolutional code definition parameters:
    - code rate,
    - code generation vectors,
    - code constraint length.

- The survivor memory word length (RAM)
- The initial path metric for state 0,
- Parallel or serial (reverse or correct order) data output format.

FUNCTIONAL DESCRIPTION

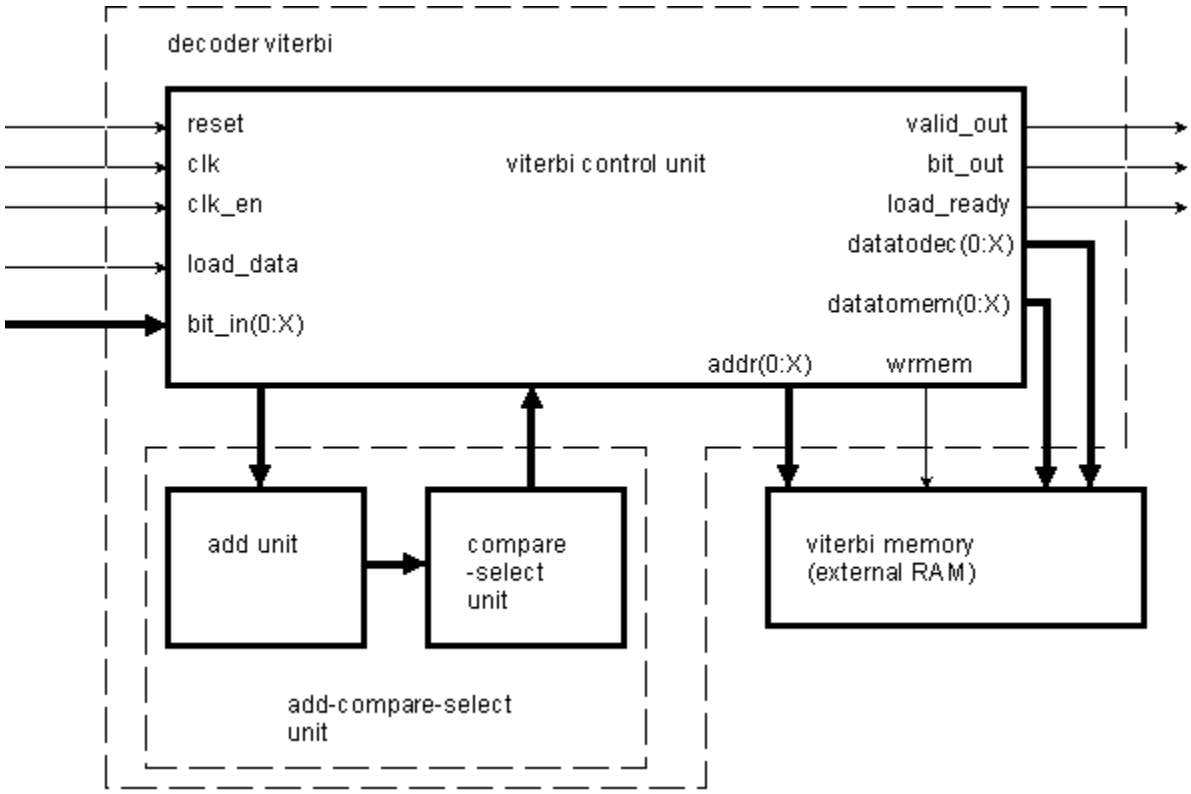

Figure 2. Viterbi Decoder Block Diagram.

The Viterbi core is partitioned into modules as shown in figure 2 and described below:

Add Compare Select (ACS) Unit

The ACS unit calculates the path metrics to find the minimum path. The ACS unit has a RADIX-4 architecture. The number of ACS units is parameterizable.

Viterbi Control Unit

The control block controls the operation of Viterbi decoder. This block handles the survivor memory management. The state-machine controls the alternation of reading new branch metrics and trace back. During trace back control unit reads the decision values from external memory and outputs the decoded bits. It reconstructs the actions in the reversed order by updating the state-register with a decision value pointed by the former state value but the decoded bits are output in **correct** order.

Viterbi Memory

Viterbi memory is a RAM memory, which stores the trace back values during calculation.

INTERFACE

Symbol

Figure 3 shows Viderbi Decoder core symbol.

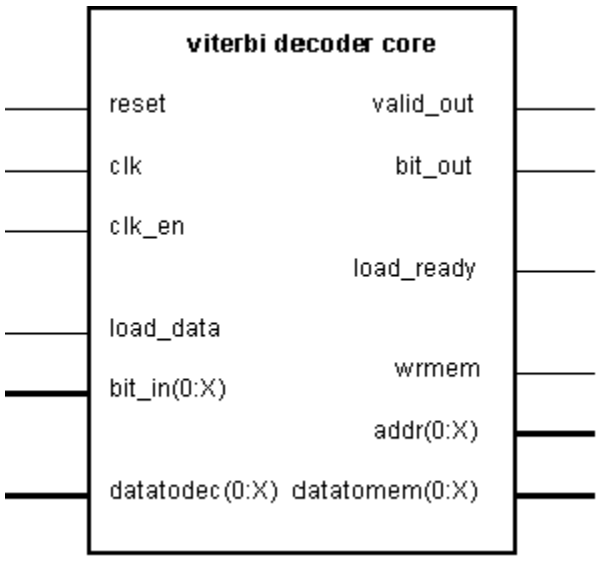

Figure 3. Decoder Viterbi core symbol.

Signal description

The descriptions of the core signals are represented in the below table.

SIGNAL	TYPE	DESCRIPTION
clk	input	Global clock
clk_en	input	Clock enable, active high
reset	input	Asynchronous reset, active high
load_data	input	Enables data loading, active high
bit_in(0:X)	input	Input values, the width depends on the code parameters
datatodec(0:X)	input	Data from external memory
valid_out	output	Valid output data, active high
bit_out	output	Decoded output bit
load_ready	output	Ready for data, active high
wrmem	output	Write enable to external memory, active high
addr(0:X)	output	Address to external memory
datatomem(0:X)	output	Data to external memory

Typical Core Interconnection

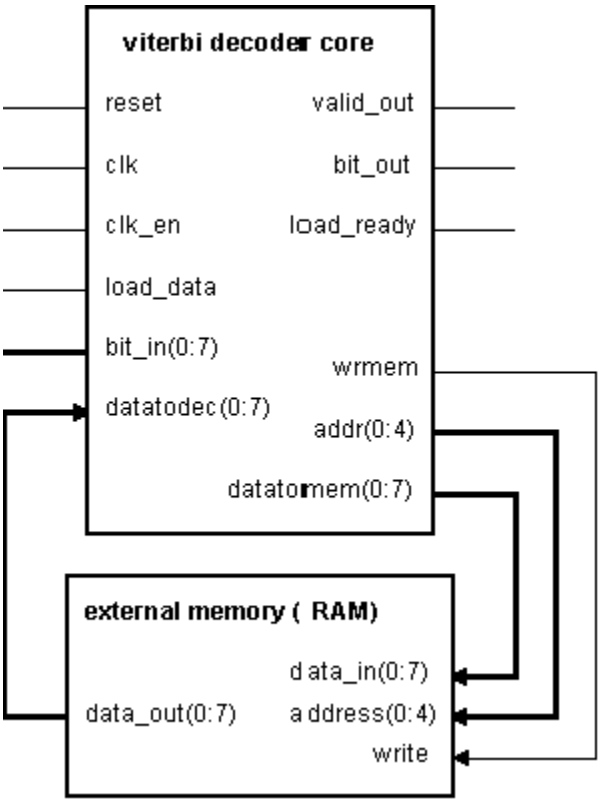

Figure 4. Typical Decoder Viterbi core interconnection with external memory.

Components:

Viterbi decoder core

RAM - external data memory 32 bytes

-

IMPLEMENTATION DATA

Performance

The following table illustrates the VITERBI DECODER core performance in Xilinx VIRTEX™, Xilinx 4000 series, Xilinx Spartan™ and Altera Flex6000 devices.

Target device	**XC4013XLBG256-09**	**XCV300BG352-5**	**S30VQ100-3**	**EPF6024ATC144-1**
Area	Number of CLBs: 383	Number of Slices: 544	Number of CLBs: 383	LCs: 1355
System clock fmax	23.938MHz	45.754MHz	11.402MHz	22.57MHz

Results obtained for the parameters in the table below.

Parameter	Value
Number of states in trellis	16
Number of bits to represent transition values	8
Length of the trace back	32
Length of the received burst	5
Initial path metric for state 0	-4
Survivor memory word length	8